High-resolution, high-speed CMOS image sensors for biomedical, industrial and semiconductor applications

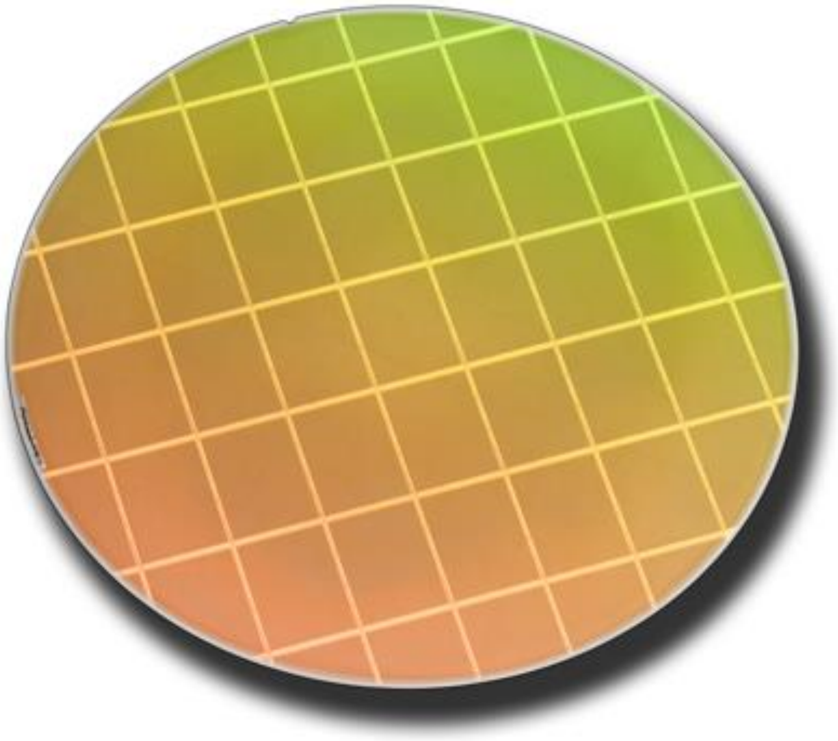

Figure 1. Photo of a CMOS wafer with the intraoral sensor developed by IMASENIC.

CMOS image sensors (CIS) are today the main imaging technology, having overtaken charge-coupled devices (CCDs) already a few years ago. CIS represents a growing fraction of the total semiconductor market, comprises 3.9% of the total market in 2021, equivalent to 21.3BUSD. Traditionally, the growth of the CIS market, both in terms of technology progress and in terms of commercial value, has been driven by the mobile phone market. Mobile phones are still the main application for CIS, but their share of market is slowly reducing. From 2020 to 2021 it went down from 68% to 63% and its decline is expected to continue. However, the CIS market is continuing to grow. This growth is now coming mainly from other application like industrial robots, automotive, surveillance, and medical equipment.

In automotive, cameras are introduced for different applications: e-mirrors, in-cabin monitoring, viewing and for autonomous driving. The market average of cameras per vehicle was 3 in 2021 with top of the range vehicle having up to 12 cameras. By 2027 these two figures are expected to increase to 5 and 20 for the market average and top of the range respectively.

In medical imaging, the CAGR in the next years is expected to be at a high level of 7.7%. CIS are found in many medical systems. Endoscopy is one of the applications. This requires very small pixels so that cameras with a good resolution can be fitted in the small size of an endoscope head without causing any discomfort to the patients. Due to the small size of the sensor and despite the large number of endoscopes, the size of the semiconductor market for this application ends up being quite small in relative terms. The growth (and volumes) in medical imaging for the CIS industry comes mainly from the large sensors that are used in equipment used for X-ray imaging.
IMASENIC is a fabess semiconductor company and develops sensors for this market, based on its innovative IPs. Founded in 2017, it is based in Barcelona and holds the European seal of Innovative SME since 2020. IMASENIC develops custom CMOS image sensors for customers around the world. Its first product was a fine pitch sensor for intraoral dental imaging. For this product, IMASENIC developed an innovative pixel which allows to achieve a very high dynamic range (HDR), as well as doing noiseless charge binning. In binning the HDR function is preserved. The sensor integrates column-parallel programmable gain amplifiers (PGA) and analogue-to-digital converters (ADC). It also integrates all the digital sequencer and biasing, all being fully programmable through an SPI interface. The sensor is of the type “camera-on-a-chip” making possible the integrate of very compact intraoral modules, see Figure 2. The sensor is now in volume production, and it exists in a variety of sizes, from a 1.9

Megapixel (size1) to a 9.2Megapixel, the latter being used for extraoral panoramic imaging.

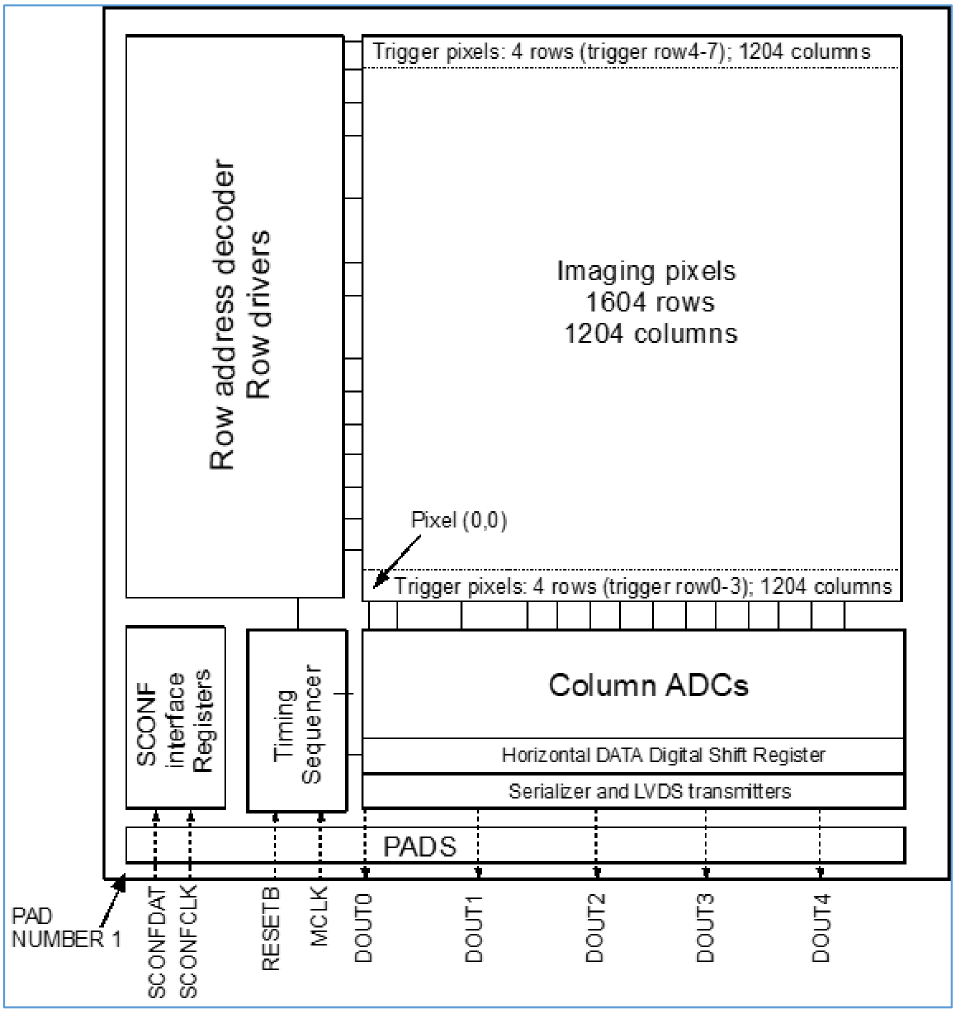

Figure 2. Floorplan of the intraoral dental sensor. It integrates all controls, hence being like a full camera on a chip.

The creation of a family of a sensor starting from a unique mask set is possible thanks to the use of a technique called “stitching”. Stitching has been used since the 90s in the semiconductor industry to make dies larger than the mask reticle. Dies as large as a single wafer can be manufactured. How does stitching work? In standard VLSI manufacturing the image of a reticle is repeated across a wafer. The size of the reticle can vary from one manufacturer to another one, but it is always of the order of 20-30mm in both directions. This is much smaller than the size of a wafer in a modern technology, generally having a diameter of 200 or 300 mm. In order to make dies as large as a wafer, it is then necessary to play some tricks on the step-and-repeat procedure. The most common way of making large dies is to partition the reticle as indicated here below. The reticle is made up of the pixel block A, the right and left (R and L) and top and bottom (T and B) blocks and the four corner blocks (1, 2, 3 and 4). At every step, the reticle is only partially exposed and the final result is the sensor shown on the right of the Figure 3.

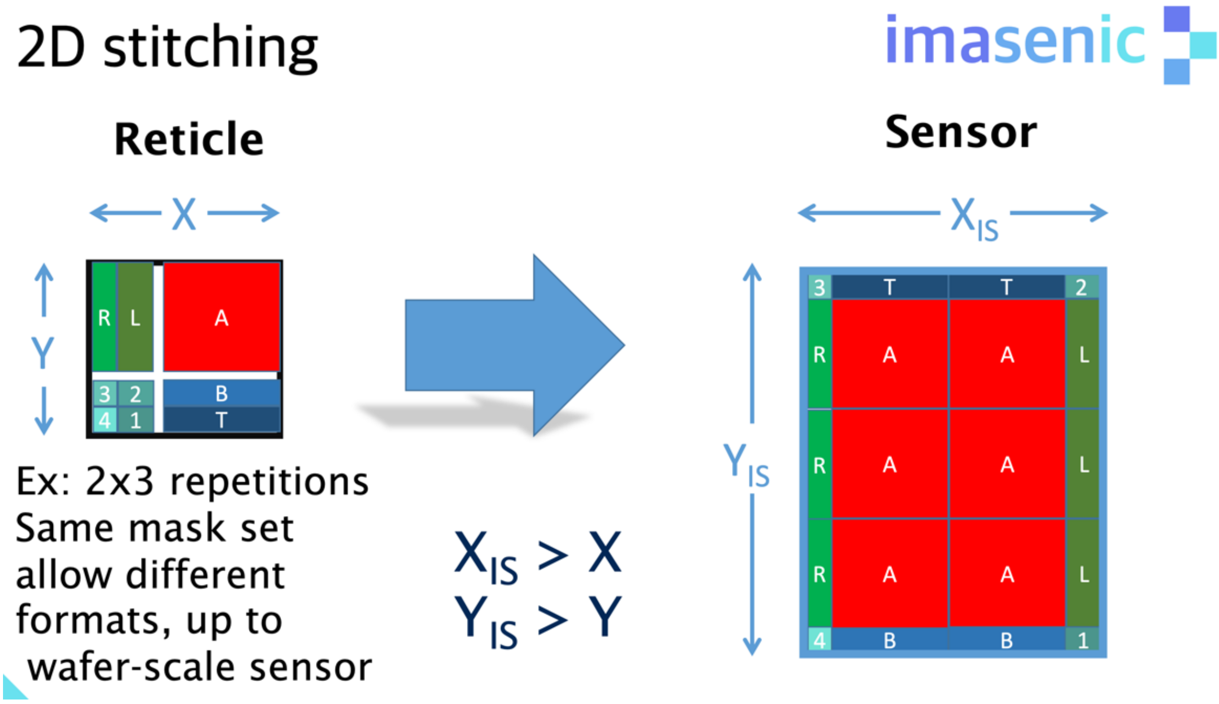

Figure 3. Reticle plan for a stitched sensor.

In its continuous commitment to improve the performance of its image sensors, IMASENIC has now developed the IMA300 series, whose first element is the sensor IMA302 (Figure 4), a 11.6Mixel sensor with a pixel pitch of 8 µm. The sensor features simultaneous low noise at 1.5 e- rms and high dynamic range, in excess of 92.7 dB, thanks to a full well of more than 65,000 electrons. The sensor works at 30 fps, which makes it suitable for application where video streaming is needed. The sensors in the IMA300 family are backside illuminated in order to achieve high quantum efficiency (QE). Depending on the applications, the quantum efficiency can be optimised for visible light applications, with a QE in excess of 90% in visible, or for deep ultraviolet applications, with a QE higher than 40% at 193nm. IMA302 will be commercially available in Q2 2024. An evaluation and a development kit will also be available. Planned in this series is also the IMA304, which is a medium format, 69.5Mpixel sensor. Other formats, with the same electro-optical performance, are available on request.

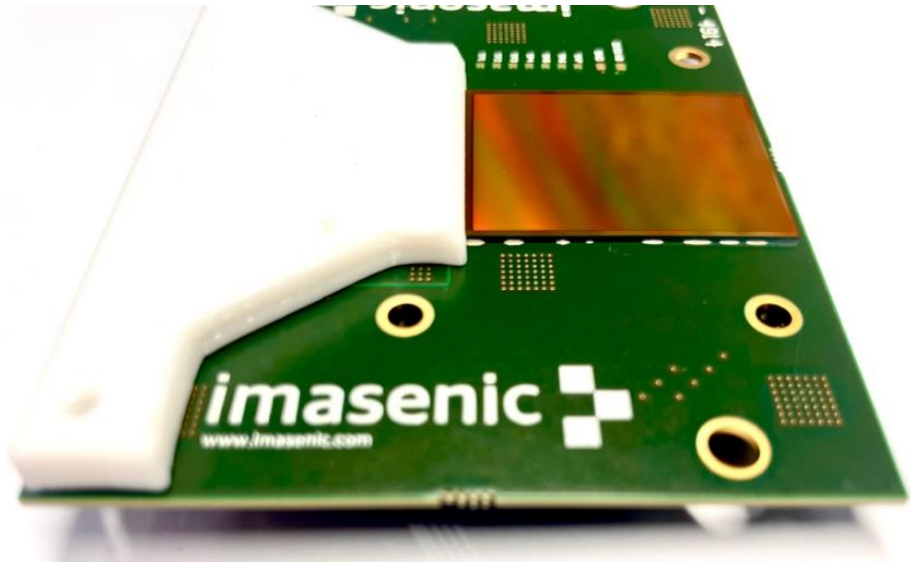

Figure 4. Photo of the IMA302 low noise, high dynamic range CMOS image sensor developed by IMASENIC

As mentioned here above, stitching allows to make sensors as large as an entire wafer. Because of the way it is done, see Figure 3, there are some additional constraints on the design with respect to smaller, non-stitched designs. The readout lines from the pixels to the periphery are very long, spanning over the entire wafer, thus the associated parasitic elements are correspondingly large, thus challenging the readout speed of sensors of this type. On top of this, as each wafer has only one sensor, special care has to be taken in the design of the sensor so that a high fabrication yield is achieved. In IMASENIC we have a long experience in designing large area sensors and this unique know-how enables high yield design of wafer-scale sensors. Over the topic of achieving high-speed, this is addressed by the design of our sensor Sagara1212. The numbers in the name indicates the size of the sensor in centimetres. This sensor takes on an entire 200 mm diameter wafer. It is designed in a 180nm technology. IMASENIC developed the wafer-scale image sensor as well as the high-speed readout electronics for the cameras where the sensor is integrated. The sensor was developed for direct detection of electrons in a transmission electron microscope It features 4 millions of radiation-hard pixels. The floorplan is similar to the one shown here above in Figure 2. It has 24,576 column-parallel ADCs with variable resolution from 6 to 10 bits. At 8-bit resolution, it achieves over 5000 frames per second, equivalent to a pixel rate of 22 billion pixels per second. Until now, this type of pixel rate was only possible in much smaller sensors. Thanks to our proprietary technology, we could go beyond this limitation. The overall data rate is in excess of 200 Gbps. A photo of the sensor is shown in the Figure 5 here below.

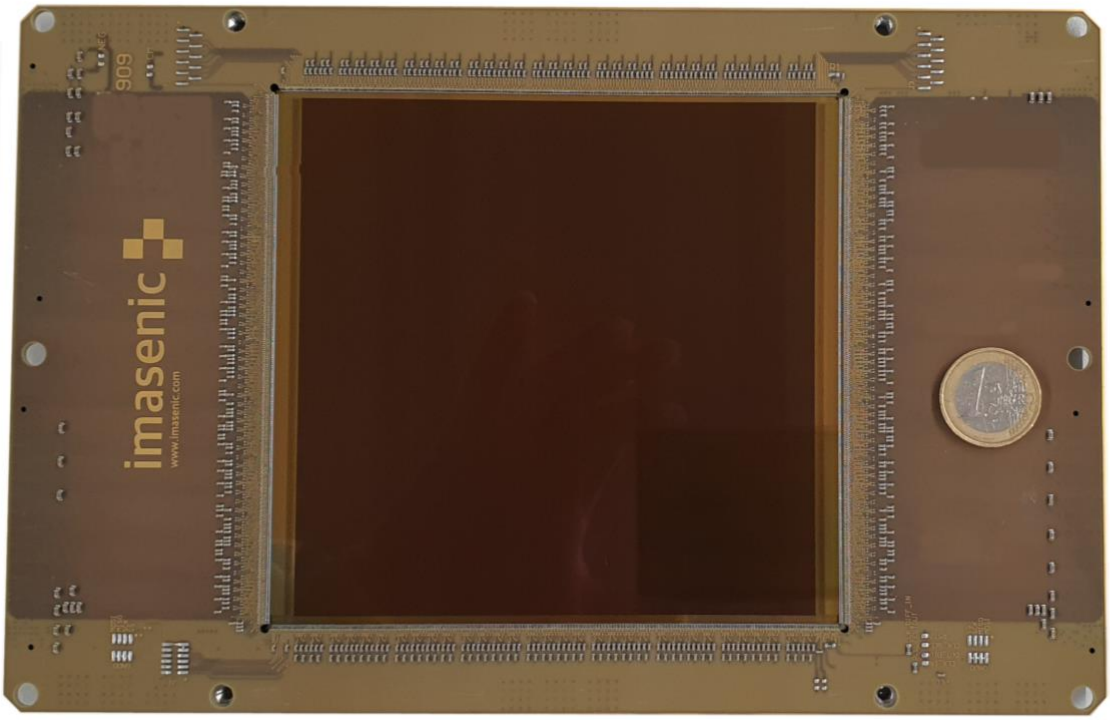

Figure 5. Photo of the Sagara1212 high-speed, wafer-scale sensor. A 1-euro coin is shown to give the scale of the sensor.

For some X-ray applications, like in medical, industrial and non-destructive tests in the semiconductor industry, the field of view is even larger than one CMOS wafer. An imaging module needs to be comprised of more than one wafer-scale sensor. In order to avoid dead space in between sensors, special design techniques are needed to achieve what is called a “3-side buttable” sensor, i.e. a sensor which has less than half a pixel dead area on 3 sides. IMASENIC has developed IP which allows to fabricate 3-side buttable sensors while achieving high readout speed and high fabrication yield. This design paves the way to new developments in high-speed, wafer-scale detectors.